REMARKS

The Official Action dated June 7, 2005 has been received and its contents carefully noted. In view thereof, claim 15 has been canceled and claims 12 and 21 have been amended in order to better define that which Applicants regard as the invention. Accordingly, claims 12-14 and 16-21 are presently pending in the instant application.

With reference now to the Official Action and particularly page 2 thereof, claims 15 and 21 have been rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

With respect to claim 15, as can be seen from the foregoing amendments, this claim has been canceled and consequently further discussion with respect thereto is no longer believed to be warranted.

With respect to claim 21, the Examiner states that the structure being claimed is unclear in that the side faces of the chips have not been claimed to reveal the location of the various chip faces recited and the location relative to each others side of the chip. In this regard, as can be seen from the foregoing amendments, dependent claim 21 has been amended in order to clarify that which Applicants regard as the invention. Accordingly, it is respectfully submitted that Applicants' claimed invention as set forth in dependent claim 21 now clearly recites the side faces referred to therein as well as the particular location relative to one another. Therefore, it is respectfully submitted that claim 21 is now in proper formal condition for allowance.

Further on page 2 of the Office Action claims 12-14 and 16-20 have been rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 1-4 of U.S. Patent No. 6,509,638 in view of Jones et al., Applicants'

prior art Fig. 6 and Koshio. This rejection is respectfully traversed in that U.S. Patent No. 6,509,638 when taking alone or in view of Jones et al., Applicants' prior art Fig. 6 and Koshio fails to disclose or remotely suggest that which is presently set forth by Applicants' claimed invention.

As the Examiner notes, claims 1-4 of U.S. Patent No. 6,509,638 are not identical to that of the presently claimed invention; however, the Examiner is of the position that because the stacked chip structure recited in the claims of the instant application recites similar features to those recited in the patented claims except that the claims of this invention recite a third chip stacked in combination with the first and second chips recited in the patented claims, the present invention would be obvious in view of the teachings of Jones et al., Applicants' prior art Fig. 6 and Koshio. However, this is clearly not the case.

The present invention is directed to a structure wherein two chips are positioned under a single chip with the two chips being a first semiconductor chip and a second semiconductor chip having a circuitry side and a non circuitry side that face each other vertically and each of which is electrically connected to the wiring board by way of raised electrodes, the circuitry side of the first and second chips facing the principle surface of the wiring board. Furthermore, independent claim 12 recites that the third semiconductor chip which has a circuitry side and a non circuitry side includes external electrodes on the circuitry side thereof wherein the non circuitry side of the third semiconductor chip is secured to the non circuitry side of the first semiconductor chip and the non circuitry side of the second semiconductor chip, the electrodes of the third semiconductor chip are connected to the wiring board by way of metal fine wires and the external electrodes are disposed so as not to overlap with the raised electrodes. These features are clearly neither disclosed in nor suggested by the prior art of record.

As the Examiner can appreciate, independent claim 1 of U.S. Patent No. 6,509,638 is directed to the structured illustrated in Fig. 1 of the present application which includes first and second semiconductor chips having non circuitry sides facing one another with the first semiconductor chip being electrically connected to the wiring board by way of raised electrodes and the second semiconductor chip being electrically connected to the wiring board by way of metal wires. Clearly, the structure illustrated in Fig. 1 fails to include first and second semiconductor chips underlying a third semiconductor chip as recited in the present independent claim 12. Furthermore, Applicants' admitted prior art set forth in Fig. 6 likewise fails to overcome this shortcoming. With respect to the teachings of Jones et al., this reference merely discloses the stacking of semiconductor chips with respect to one another; however, nowhere is it disclosed that first and second semiconductor chips are to be positioned between a wiring board and a third semiconductor chip with each of the first and second semiconductor chips being electrically connected to the wiring board by way of raised electrodes while the third overlying semiconductor chip is electrically connected to the wiring board by way of metal fine wires.

Likewise, the patent to Koshio similarly fails to disclose such a structure.

Furthermore, as the Examiner can appreciate, the claimed invention set forth in U.S. Patent No. 6,707,143 has been deemed patentably distinct from the claimed invention set forth in U.S. Patent No. 6,509,638 and consequently, it is respectfully submitted that the present invention set forth in claims 12-14 and 16-21 is likewise patentably distinct from the invention claimed in U.S. Patent No. 6,509,638. With the present invention, Applicants have not simply increased the number of chips but rather have mounted one chip on two chips in a particular manner wherein the number of layers in the substrate decreases as the wiring density decreases. In this regard, the present invention results in a slimmed down substrate

with reduced costs. Accordingly, it is respectfully submitted that Applicants' claimed invention as set forth in independent claims 12 as well as those claims which depend therefrom patentably distinguishes from the claimed invention set forth in U.S. Patent No. 6,509,638 when taken alone or in view of the secondary references cited by the Examiner. Therefore, it is respectfully submitted that Applicants' claimed invention as set forth in independent claim 12 as well as those claims which depend therefrom clearly distinguish over the prior art of record and are in proper condition for allowance.

With reference now to page 4 of the Office Action, claims 12-21 have been rejected under 35 U.S.C. §101 as claiming the same invention as that of claims 1-10 of prior U.S. Patent No. 6,707,143. This rejection is respectfully traversed in that the invention set forth in independent claim 12 as well as those claims which depend therefrom is clearly patentably distinct from claims 1-10 of U.S. Patent No. 6,707,143.

Specifically, the invention claimed in U.S. Patent No. 6,707,143 is directed to the features illustrated in Fig. 4 of the present application and recite a semiconductor device including a wiring board, a first semiconductor chip having a circuitry side and a non circuitry side the first semiconductor chip being electrically connected to the wiring board by way of raised electrodes and the circuitry side of the first chip facing the principle surface of the wiring board, a second semiconductor chip which has a circuitry side and non circuitry side including external electrodes on the circuitry side thereof as well as a third semiconductor chip which has a circuitry side and non circuitry side with external electrodes included on the circuitry side thereof. The non circuitry sides of the second and third semiconductor chips are secured to the non circuitry side of the first semiconductor chip and the external electrodes of the second and third semiconductor chips are connected to the wiring board by way of metal fine wires while the external electrodes are disposed so as not

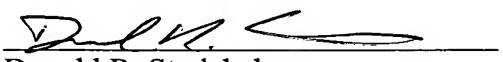
to overlap the raised electrodes. As the Examiner can readily appreciate, this is not the same or even essentially the same structure as that of the instant claims.

U.S. Patent No. 6,707,143 recites an invention wherein two chips are mounted on a first chip and the external electrodes do not overlap with the raised electrodes in the perpendicular direction and the two chips are stacked on the first chips. To the contrary, the present invention recites a device wherein two chips are mounted on and electrically connected to the wiring board while a third chip is positioned and secured to a non circuitry side of each of the first and second chips and is electrically connected to the wiring board by way of fine metal wires. The present invention is certainly not essentially the same as that claimed in U.S. Patent No. 6,707,143. Accordingly, just as U.S. Patent No. 6,707,143 is patentable distinct from U.S. Patent No. 6,509,638, the present invention set forth in independent claim 12 as well as those claims which depend therefrom is patentable distinct from the invention claimed in each of U.S. Patent No. 6,509,638 as well as 6,707,143. Therefore, it is respectfully submitted that Applicants' claimed invention clearly distinguishes over the invention claimed in U.S. Patent No. 6,707,143 and is in proper condition for allowance.

Therefore, in view of the foregoing it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 12-14 and 16-21 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,



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